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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,190	06/19/2001	Sunil K. Jain	219.39488X00	9925

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	15

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,190	JAIN ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/24/2004 has been entered.

Claims 1-43 are pending.

Response to Amendment

The examiner acknowledges the amendments to Claims 1, 14, 18, 28, 33, 37 and 42.

Response Re: Claim Rejections - 35 USC § 102

1. In response to Claims 1-4, 14-17, 18-21 and 42, and after amendment to Claims 1, 14, 18, 28, 33, 37 and 42, the applicant argues that Gohringer does not teach or suggest the claimed features of the applicant; specifically, Gohringer does not teach or suggest applying a test signal with analog, digital, and differential components. The examiner agrees, and therefore withdraws the rejection of Claims 1, 14, 18 and 42. And because the subject claims are allowable over the cited art, Claims 2-13, 15-17, and 19-27, which depend from Claims 1, 14 and 18 are also withdrawn.

Response Re: Claim Rejections - 35 USC § 103

2. In response to Claims 28-31, 33, 34, 36, and 37-41, and after amendment to Claims 1, 14, 18, 28, 33, 37 and 42, the applicant argues that the references of Sauer and Grochowski fails to teach or suggest the claimed features of the applicant; specifically, the refernces do not teach or suggest applying a test signal with analog, digital, and differential components. The examiner agrees, and therefore withdraws the rejection of Claims 28, 33 and 37. And because the subject claims are allowable over the cited art, Claims 29-32, 34-36, and 37-41, which depend from Claims 28, 33 and 37 are also withdrawn.

The examiner reiterates at this time that Claims 1-42, withdrawn as detailed above, stand pending in this action below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 14, 8, 18, 24 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and in view of Deome et al., U.S. Patent No. 6512989.

As per Claims 1, 14, 18 and 42:

Organ et al. teaches a method of testing, including a programmable medium, an electronic device (see Abstract and column 34 line 51) based on the apparatus, said method and apparatus comprising: applying to the electronic device input test signals

(see Abstract) having an analog signal component (FIG.1 22), a digital signal component (FIG.1 20), and a differential signal component (column 8 lines 15-16); and monitoring the response of the electronic device on a tester receiver to obtain digital data (column 8 lines 65-68 and column 8 line 1), and processing the digital data (column 33 lines 60-62) and comparing the processed digital data (column 8 lines 10-11). And as per column 33 lines 30-42, analog and digital testing is performed independently simultaneously. Organ however fails to teach specifically the analog monitoring and processing of the DUT. In an analogous art, Deome et al. does teach these features. Deome et al. teaches monitoring the response of the electronic device on a differential monitoring device to obtain analog data (column 10 lines 9-49); processing the analog data (column 10 lines 9-49 and column 12 lines 50-54), comparing the processed analog data evaluating the compared data (column 10 lines 9-49); and evaluating the electronic device based on the evaluated data (column 11 lines 31-43). Deome et al., in column 3 lines 16-38 relates the advantages of the invention as being a way to test both digital and analog functions on a DUT with one control pattern. And one with ordinary skill in the art at the time of the invention, motivated to apply the advantages of Deone et al. as suggested, would combine the two references, and so the claims are rejected.

As per Claims 8 and 24:

Organ et al. further teaches the method as claimed in claim 1 and 18, wherein processing the analog data and the digital data comprises determining the rise time and the fall time of a signal in the response of the electronic device (Organ et al., column 32

lines 46-56). And in view of the previously mentioned motivation, the claims are rejected.

4. Claims 9 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and Deome et al., U.S. Patent No. 6512989 as applied to Claim 1 and 18 above, and further in view of Grochowski et al., "Integrated Circuit Testing for Quality Assurance in Manufacturing: History, Current Status, and Future Trends", 1997, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 44, No. 8, August 1997. Grochowski et al. teaches the method as claimed in claim 1, wherein processing the analog data and the digital data comprises determining the ranges of rise times and of fall times within a signal in the response of the electronic device (Grochowski et al., page 626, column 2 6th paragraph). And, on page 610 column 2 of Grochowski et al., the advantages of driving down the cost of testing and minimizing the number of bad devices are an object of the paper. Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made, motivated as suggested by both Sauer et al. and Grochowski et al., to combine the references above, and so the claims are rejected.

5. Claims 10-13, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and Deome et al., U.S. Patent No. 6512989 as applied to Claim 1 above, and further in view of Information relating to differential oscilloscope usage, interfaces using GPIB, and eye diagram outputs; http://www.tek.com/site/ps/0,,55-16615-SPECS_EN,00.html (previously referenced in the examiner's 1st office action). This reference is a product information

bulletin published by Tektronix Corporation describing RT-Eye™ Serial Data Compliance and Analysis software related to the TDS6000 and TDS7000 digital oscilloscope, which is marketed by the company. Included in this product is the capability to; monitoring an eye diagram, determining a rise time and a fall time of a signal in the eye diagram, determining the ranges of rise times and of fall times within a signal in eye diagram, and monitoring boundary conditions in the eye diagram (see product bulletin). The bulleting boasts of real time eye rendering with custom report generation. One with ordinary skill in the art at the time of the invention, motivated by this bulletin, would combine the references, and so the claims are rejected.

6. Claims 2, 3, 4, 15, 16, 17, 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and in view of Deome et al., U.S. Patent No. 6512989 as applied to Claims 1, 14 and 18 above, and further in view of Gohringer, U.S. Patent No. 5909186.

As per claims 2, 15, and 19:

Gohringer teaches a method, system, and apparatus wherein analog data feeds back for use in processing digital inputs, and digital data feeds back for use in processing analog inputs. In his claim 4, he takes a digital counter based on an digital signal received from the DUT, converts it to analog value, and applies the analog signal to the analog input of the DUT. In claim 15 he takes a digital value based on an analog signal received from the DUT, and applies the digital value, which has been modified, to the digital input of the DUT. And Gohringer, in column 4 lines 66-67 and column 5 lines 1-2, boasts that the invention provides a quicker and more cost-effective apparatus and

method of testing mixed-signal devices. One with ordinary skill in the art at the time of the invention, motivated by Gohringer, would apply all references mentioned, and so the claims are rejected.

As per claims 3, 4, 16, 17, 20, and 21:

Gohringer compares and evaluates the outputs from the DUT and re-iterates the test process with different input values until testing is stopped by an error or reaching a predetermined value. Gohringer claim 15 teaches this by claiming the following steps: (1) providing a signal, (2) performing test operation, (3) converting DUT output, (4) incrementing count until equal, (5) evaluating DUT, (6) repeating all until error. And one with ordinary skill in the art at the time of the invention, motivated by Gohringer as previously recited above, would apply all references mentioned, and so the claims are rejected.

7. Claims 5, 6, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and Deome et al., U.S. Patent No. 6512989 as applied to claims 4 and 21 above, and further in view of Sauer et al. U.S. Patent 5951704. Wherein Organ et al. teaches a mixed signal tester, with applied signals that can be varied through a feedback loop with the monitoring unit(FIG.3), the reference does not teach varying frequency and level of the input signals to the DUT as in above claims 5, 6, 22, and 23. However, Sauer et al., in an analogous art, further teaches, "...various parameters are specified such as frequency, waveform, delay time and amplitude of the test signal to be applied to each terminal of the semiconductor device...". And Sauer et al., in column 3 lines 23-50 recites

advantages of the invention to be means for evaluating and debugging test protocols without the use of hardware. One with ordinary skill in the art at the time of the invention, motivated by Sauer et al., would combine the referenced art, and so the claims are rejected.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and in view of Deome et al., U.S. Patent No. 6512989 as applied to Claim 1, and further in view of G. Cauffet et al., Digital Oscilloscope Measurements in High Frequecncy Power Electronics, IEEE, reference 0-7803-0640-6/92, pages 445 - 447. Whereas Organ et al. teaches the tester using standard tester measurement hardware (FIG.1), Cauffet et al. explicitly discloses "associating a digital oscilloscope for acquisition, to a work station for control, corrections, mathematical processing, and presentation" (paragraph 3), in measurements of high frequency power electronics. And Cauffet et al. cites the evolving problem of more complicated electrical measurements being required by modern circuits in the Abstract of the paper, and wherein the differential oscilloscope has become a major investigation tool. One having ordinary skill in the art at the time the invention was made would have been motivated by the advantage described by Cauffet et al., and one would have attached a digital oscilloscope to a tester as in Organ et al., and so the claim is rejected.

9. Claims 28–31, 33-34, 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, Deome et al., U.S. Patent No. 6512989, Sauer et al., U.S. Patent No. 5951704, and Grochowski et al., "Integrated Circuit Testing for Quality Assurance in Manufacturing: History, Current Status, and

Future Trends", 1997, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 44, No. 8, August 1997.

As per all of the above-mentioned claims, Organ et al. and Deome et al. teach the equipment characteristics of the virtual test system but the references do not tech the emulator. In analogous art, Sauer et al. substantially teaches a method and a system for programming an emulator (see Abstract), which encompasses virtual hardware to generate test signals, a virtual device attached to the virtual test head, and a device emulator which outputs to an emulated comparator (column 2 lines 23-68 and column 3 lines 1-50). The result is a totally virtual test system for developing the present tester protocol and changes thereof, tester hardware changes, device design and modification, all without using the hardware of the test system (column 9, lines 42 – 53, and column 10, lines 4 – 67). And Sauer et al., in column 3 lines 23-50 recites advantages of the invention to be means for evaluating and debugging test protocols without the use of hardware. But not explicitly disclosed is the use of a general-purpose computer in the Sauer et al. invention, as claimed in this application.

However, in an analogous art, Grochowski at al., is quoted in the publication as follows; "Computer models that emulate the ATE are being developed to be incorporated into the same CAD tools used during the design phase. This will allow the test engineer to exercise the model for DUT (i.e., SPICE or HDL) within an emulated test environment." (page 619 line 6). This statement specifically points to a general-purpose computer driven system. And, on page 610 column 2 of Grochowski et al., the advantages of driving down the cost of testing and minimizing the number of bad

devices are an object of the paper. Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made, motivated as suggested by both Sauer et al. and Grochowski et al., to combine the references above, and so the claims are rejected.

10. Claims 32, 35 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and in view of Deome et al., U.S. Patent No. 6512989, Sauer et al., U.S. Patent No. 5951704, and Grochowski et al., "Integrated Circuit Testing for Quality Assurance in Manufacturing: History, Current Status, and Future Trends", 1997, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 44, No. 8, August 1997 as applied to Claims 28, 33, and 37 above, and further in view of G. Cauffet et al., Digital Oscilloscope Measurements in High Frequecncy Power Electronics, IEEE, reference 0-7803-0640-6/92, pages 445 - 447. Whereas Organ et al. teaches the tester using standard tester measurement hardware (FIG.1), Cauffet et al. explicitly discloses "associating a digital oscilloscope for acquisition, to a work station for control, corrections, mathematical processing, and presentation" (paragraph 3), in measurements of high frequency power electronics. And Cauffet et al. cites the evolving problem of more complicated electrical measurements being required by modern circuits in the Abstract of the paper, and wherein the differential oscilloscope has become a major investigation tool. One having ordinary skill in the art at the time the invention was made would have been motivated by the advantage described by Cauffet et al., and one would have attached a digital oscilloscope to a tester as in Organ et al., and so the claims are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

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Guy J. Lamarre for

Albert DeCady
Primary Examiner